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VLSI Technology for Smaller, Cheaper, Faster Return Link Systems

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ABSTRACT

Very Large Scale Integration (VLSI) Application-specific Integrated Circuit (ASIC) technology has enabled substantially smaller, cheaper, and more capable telemetry data systems. However, the rapid growth in available ASIC fabrication densities has far outpaced the application of this technology to telemetry systems. Available densities have grown by well over an order magnitude since NASA's Goddard Space Flight Center (GSFC) first began developing ASICs for ground telemetry systems in 1985. To take advantage of these higher integration levels, a new generation of ASICs for return link telemetry processing is under development. These new submicron devices are designed to further reduce the cost and size of NASA return link processing systems while improving performance. This paper describes these highly integrated processing components.

1. INTRODUCTION

The rapid growth of chip fabrication densities has had a tremendous positive impact on NASA telemetry data systems. Each year, new data system implementations are getting smaller, cheaper, and more powerful due to the availability of higher integration components developed through improved VLSI fabrication processes. For ground telemetry systems, many of these components are the latest standard commercial microprocessors and solid-state memories developed for general purpose computing. Although general purpose components have improved telemetry data system implementations, even greater improvements have been gained with the addition of components developed specifically for telemetry processing.

The Data Systems Technology Division (DSTD) at NASA GSFC first began developing VLSI ASIC components for ground telemetry processing in 1985 [1]. This effort led to a series of more than a dozen different telemetry processing components implemented in silicon and Gallium Arsenide (GaAs) technologies. The high integration levels offered by these components enabled the development of VLSI-based systems that offered an order of magnitude improvement in performance, cost, and size over previous telemetry processing implementations. The inherent advantages of these systems has led to their wide spread use across a number of NASA programs. Over 100 VLSI-based telemetry systems have been deployed in support of such programs as the Small Explorer missions [2,3], Deep Space Network (DSN), Hubble Space Telescope (HST), and the Earth Observing System (EOS).

Integrated circuit technology has progressed very rapidly since the DSTD developed its first series of VLSI telemetry processing components. Many of the original ASIC components still in use were implemented in 2 micron semi-custom Complementary Metal Oxide Semiconductor (CMOS) gate array technology. This technology capable of fabricating parts with usable densities of up to 10,000

logic gates. While such levels of integration were impressive at the time, they are modest by today's standards. With available densities approaching 1,000,000 logic gates, current submicron semi-custom technologies offer an opportunity to once again improve the performance and shrink the cost and size of telemetry data systems.

To make full use of today's available VLSI densities, the DSTD is developing a new series of very high integration VLSI ASIC components for return link telemetry processing. The new ASICs are intended to integrate into a single device much of the functionality contained in current printed circuit card subsystems. This is expected to reduce system reproduction costs to well less than 20 % of the cost of previous VLSI implementations. These next generation VLSI components are targeted towards space science missions using the widely adopted packet telemetry protocols recommended by the Consultative Committee for Space Data Systems (CCSDS). However, they also offer a level of programmability and generic capability that make them useful for other missions with unique protocol formats. Efforts to date have focused on the development of three individual ASICs. One ASIC for Reed-Solomon error correction has been implemented and tested. Two more ASICs for frame synchronization and CCSDS service processing are currently in the design stage. In this paper, we first describe the functions required for CCSDS return-link processing. We then describe the architecture and key features of each of the three next generation VLSI components that implement these functions.

2. CCSDS RETURN LINK PROCESSING

In the past, telemetry formats tended to be unique for each new spacecraft. This led to the successive development of telemetry data systems for each new mission. This mission-unique development cycle led to very high costs for the acquisition and maintenance of data systems on a NASA-wide basis. To reduce these costs and to promote interoperability between ground processing elements, NASA adopted space data protocol standards outlined by the CCSDS, an international collaborative body composed of many of the world's space agencies. Most future NASA missions are now planning to use the CCSDS protocols. This yields great potential for significant cost savings across all future NASA flight and ground data systems.

Return link processing is an area of particular interest for cost savings. Systems implementing return link functions are used throughout NASA in ground stations, control centers, science data processing facilities, spacecraft verification equipment, compatibility testing, and launch support facilities. Demand for CCSDS return link processing systems is expected to increase dramatically beyond current uses with the advent of the EOS program. Starting in 1998, the EOS will fly a series of remote sensing spacecraft to monitor the earth's environment. Many of these spacecraft will be capable of broadcasting CCSDS formatted science data directly to the user. Because of the scope of the EOS program, it is expected that there will be a large user base for direct broadcast data and, therefore, an even greater demand for cost-effective CCSDS return link processing systems.

Return link processing takes place after the acquisition, demodulation, and digitization of signals transmitted from the spacecraft. Return-link processing systems generally extract framed data from incoming serial bit streams, correct framed data, validate the protocol structures within the frame, and extract user data. Figure 1 depicts an example return link processing chain for packetized CCSDS telemetry.

Frame synchronization is the process of delineating framed data structures from the incoming serial bit stream. CCSDS telemetry uses a specific pattern to mark frame boundaries. Because space to ground transmission induces numerous types of data disturbances, NASA frame synchronizers employ sophisticated measures in searching for these markers to ensure correct synchronization of data.
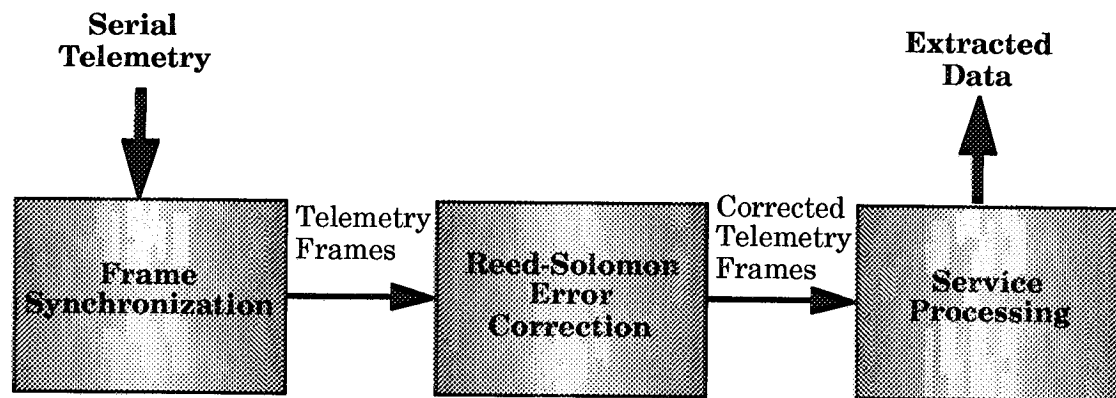
Figure 1. Example CCSDS Return Link Processing Chain

Reed-Solomon error correction removes errors introduced during the transmission process. The CCSDS recommendations specify a very powerful block error correction code to protect internal data and protocol structures of the frame. This Reed-Solomon code is applied prior to transmission in the form of appended check symbols. The data and check symbols together represent code words that are decoded on the ground to correct transmission errors. To increase the burst error correction capability of the code, a technique known as interleaving is used. Interleaving systematically alternates the symbols of multiple code words within a frame so that when a burst error occurs, it is distributed across more than one code word.

CCSDS Service Processing demultiplexes, extracts, and validates user data from the composite stream of telemetry frames. The CCSDS protocols use data driven protocol constructs and the concept of virtual channels to assign portions of the composite stream to different spacecraft instruments. Virtual channel assignments also identify the kind of processing to be performed on the data from each instrument. To extract user data, Service Processing uses protocol constructs contained in the headers of telemetry frames to identify virtual channels and the type of processing required. Packet data types are generally the most complex data type to process because individual virtual channels can carry multiplexed streams of variable length packets from different sources. Packets are also allowed to span the frames of a given virtual channel. Therefore, packet processing requires not only locating, extracting, and validating packets in frames but also piecing together packets that cross frame boundaries.

Current VLSI-based CCSDS return link telemetry systems developed by the DSTD implement these functions on several 9U form factor VMEbus printed circuit cards. The cards are densely populated with commercial VLSI components and the DSTD's first generation ASIC components using dual sided surface mount technology and plug-in daughter card assemblies. The three next generation of ASIC components currently under development will allow integration of all these functions onto a single card. Each of these new 0.6 micron CMOS ASICs is designed to minimize the number of required supporting components. Remaining supporting components mainly consist of commercial high density memories which are expensive to implement in ASIC technology. The three next generation components, described in the following paragraphs, are known as the Parallel Integrated Frame Synchronizer chip, the Reed-Solomon Error Correction chip, and the CCSDS Service Processor chip.

3. PARALLEL INTEGRATED FRAME SYNCHRONIZER CHIP

The Parallel Integrated Frame Synchronizer (PIFS) chip is currently under development and is scheduled to be completed in summer of 1995. It is being designed using 0.6 micron CMOS gate array technology. As its name implies, the PIFS chip uses a parallel algorithm to perform telemetry frame synchronization. This is different from previous generation VLSI frame synchronizer chips which used serial processing approaches. While parallel approaches are not new, they require significantly more

logic than serial approaches. Because new VLSI processes have so greatly lowered the cost and size of logic functions, greater complexity is no longer a disadvantage.

Figure 2 depicts the expected cost, size, performance, and power advantages of the next generation frame synchronizer based on the new PIFS chip as compared to present VLSI serial implementations. Currently, the DSTD uses two different frame synchronizers to meet the full range of NASA spacecraft data rates at reasonable costs. A frame synchronizer based on lower cost CMOS technology is used for telemetry data rates up to 20 Megabits per second (Mbps) [4]. For higher data rates, a more expensive frame synchronizer based on GaAs and Emitter Coupled Logic (ECL) technology is used [5]. With operating rates up to 500 Mbps, the PIFS-based next generation frame synchronizer will replace both implementations at a lower cost. This will allow the additional logistical advantage of having one frame synchronizer that meets the full range of NASA spacecraft data rates.

Parallel Integrated Frame Sync Chip

2.2"
3.1"

6.3"
4.7"

EOS Frame Sync Card
0 - 300 Mbps
$15K per Card
> 40 Watts
0.8 μ GaAs & 1.2 μ ECL Technology

Next Gen Frame Sync
0 - 500 Mbps
$500 per Card
< 10 Watts
0.6 μ CMOS Technology

6.3"
4.7"

Standard Frame Sync Card
0 - 20 Mbps
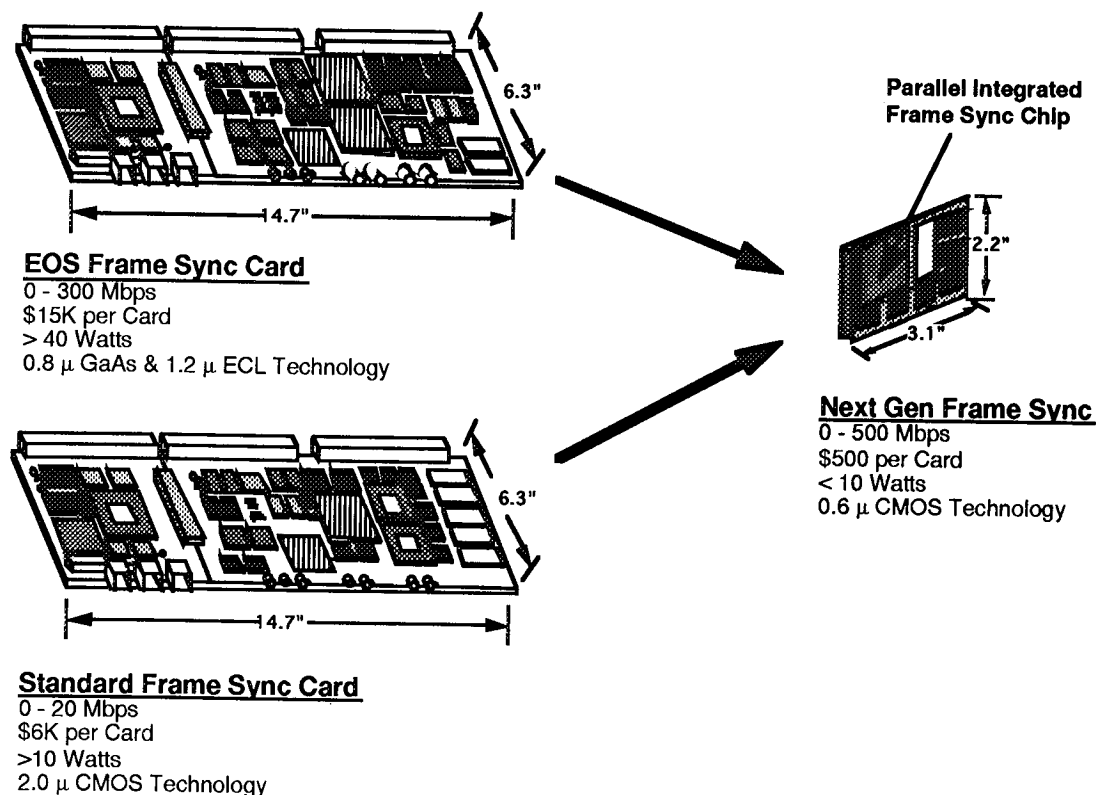$6K per Card
>10 Watts
2.0 μ CMOS Technology

Figure 2 . Next Generation Frame Synchronizer Targeted Level of Integration

A functional block diagram of the PIFS chip is shown in Figure 3. The PIFS chip is controlled by a set of internal registers that are configured through a standard microprocessor interface prior to operation. The registers allow programmability to meet the needs of many different space missions. Marker patterns, compare masks, correlator tolerances, acquisition strategy, and slip tolerances are just a few of the programmable parameters within the registers. During operation, data enters the chip in one of two ways. For very high data rates, serial data is first externally converted to byte-wide parallel data and then fed into an internal First-In, First-Out (FIFO) memory. For rates below 50 Mbps, serial data can be input directly where it is converted to parallel on-chip. The use of the FIFO memory allows the PIFS internal logic to run off a separate master clock. This feature coupled with a data-flow architecture has several advantages over previous implementations including lower latency, easier processing of nested or asynchronously blocked data, and automatic pipeline flushing. As data passes

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through the chip, correlations are performed, synchronizer locations are calculated, and data is aligned to frame boundaries before being output. The PIFS chip generally contains a superset of the functions contained in previous VLSI card-level implementations including cumulative quality accounting, time stamping, and real-time quality trailer generation. One exception is reverse data handling which becomes unnecessary with the ubiquitous future use of onboard Solid State Recorders. If compatibility with older spacecraft using tape recorders is required, this function can be accomplished by adding external Programmable Logic Devices (PLD) and random access memories. The PIFS also adds the capability to synchronize all current weather satellite formats.
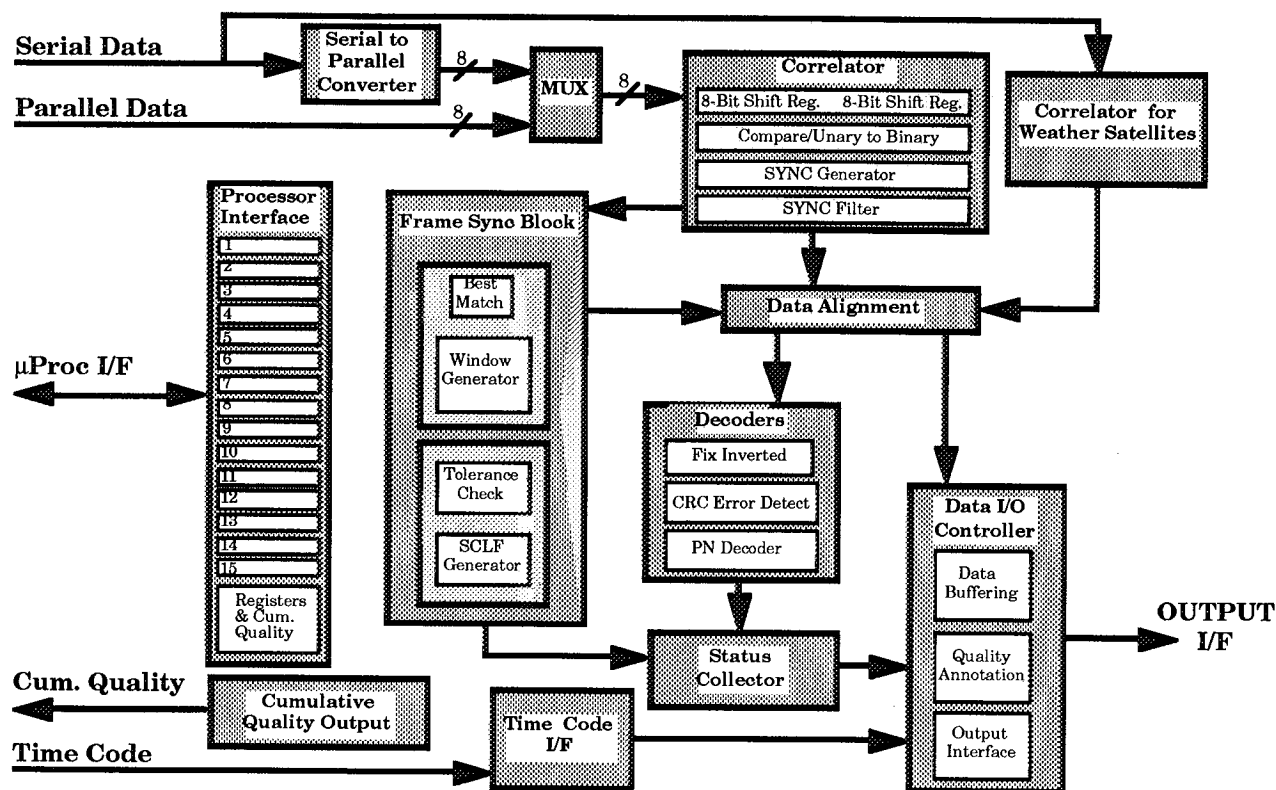

Figure 3. PIFS Chip Functional Block Diagram

4. Reed-Solomon Error Correction Chip

With over 125,000 logic gates, the Reed-Solomon Error Correction (RSEC) chip is the largest ASIC implemented to date by the DSTD. This chip, completed in February 1994, is implemented in 0.6 micron CMOS hybrid standard cell / gate array technology. The RSEC chip integrates much of the functionality currently contained on two VMEBus card subsystems. Elements of the RSEC chip include CCSDS Reed-Solomon block and header decoders, 16 KBytes of synchronous random access memory, and a pipeline of four memory controllers that perform deinterleaving, error correction, real-time quality annotation, and frame filtering and routing. The chip has been recently tested at sustained operating rates of well over 500 Mbps. This level of integration and performance coupled with the complexity of the CCSDS Reed-Solomon code make it quite possibly the most powerful error correction device in the world!

A functional block diagram of the RSEC chip is shown in Figure 4.
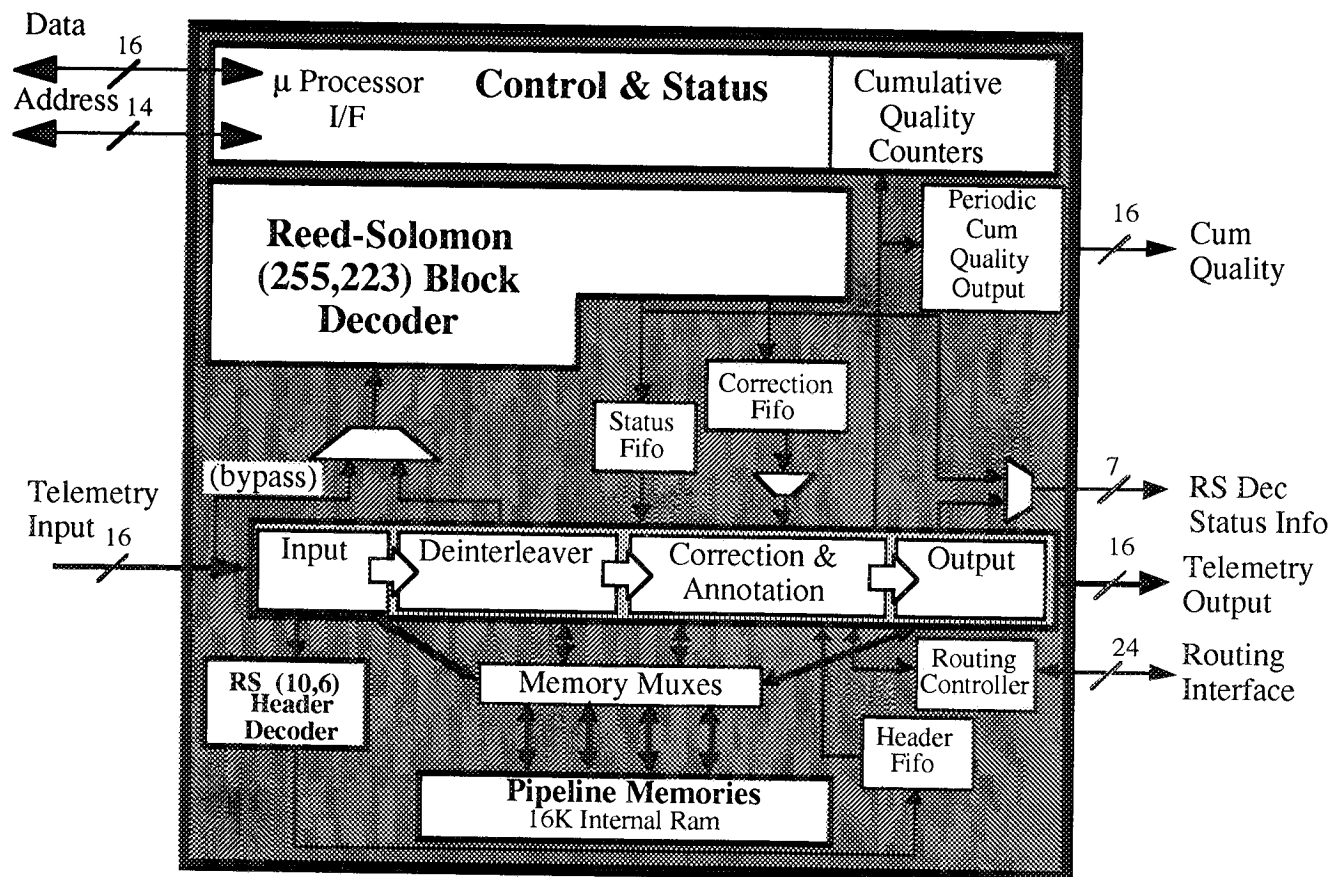
245

Data 16

Address 14

μ Processor I/F | **Control & Status** | Cumulative Quality Counters

Reed-Solomon (255,223) Block Decoder

Periodic Cum Quality Output → 16 → Cum Quality

Correction Fifo

Status Fifo

(bypass)

Telemetry Input 16

Input → Deinterleaver → Correction & Annotation → Output

7 → RS Dec Status Info

16 → Telemetry Output

RS (10,6) Header Decoder | Memory Muxes | Routing Controller

24 → Routing Interface

Header Fifo

Pipeline Memories 16K Internal Ram

Figure 4. RSEC Chip Functional Block Diagram

5. CCSDS Service Processor Chip

The CCSDS Service Processor (CSP) chip is currently under development and is expected to be completed in the summer of 1995. Implementing the CSP chip is the most ambitious of the three chip development efforts. It involves a radical change from the current Service Processor card architecture. The current Service Processor has the highest complexity of any card implemented by the DSTD. It employs three Motorola MC68040 processors, five VLSI ASIC components, over 6 MBytes of memory, and a host of commercial VLSI components. When the architecture for this card was first developed in the late 1980's [6], the CCSDS protocols were still under development. To maintain the flexibility necessary to accommodate changes in the protocols, most of the workload was implemented in software running on the three processors. Only the most generic data movement and extraction functions were placed in the VLSI ASICs.

The CCSDS recommendations have since stabilized allowing many of the current software functions to be integrated into the CSP chip. A major goal of the CSP chip is to reduce implementation cost by integrating enough functions to eliminate two of the current card's processors. Another goal of the CSP chip is to significantly increase packet processing throughput to alleviate a shortcoming in the CCSDS recommendations which allows the creation of very small packets. At even modest data rates, small packets can lead to very high packet rates. Because each packet requires a similar amount of protocol processing, bursts of small packets can quickly overload ground processing systems. Even the current Service Processor, by far the highest performance implementation to date, is easily overwhelmed by bursts of very small packets at relatively low data rates. Moving many of these functions into the CSP

chip is expected to substantially increase packet throughput. The targeted level of performance and integration of the next generation Service Processor based on the CSP chip is depicted in Figure 5.
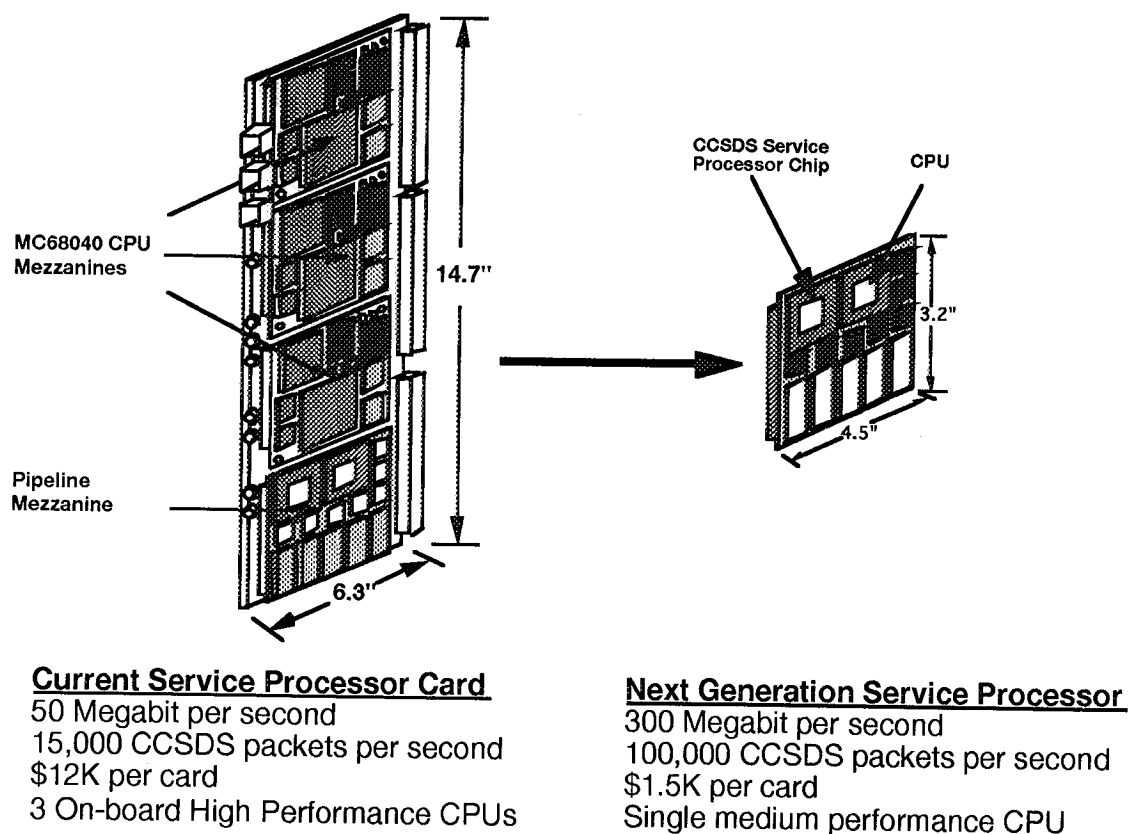

Current Service Processor Card
50 Megabit per second
15,000 CCSDS packets per second
$12K per card
3 On-board High Performance CPUs

Next Generation Service Processor
300 Megabit per second
100,000 CCSDS packets per second
$1.5K per card
Single medium performance CPU

Figure 5. Next Generation Service Processor Targeted Level of Integration

6. CONCLUSION

The development of three new VLSI ASIC components for return link telemetry processing has been discussed. These components are planned for use in the next generation of VLSI systems now under development and will find application in a number of NASA ground data systems. The RSEC chip is already planned for delivery in high performance systems that will be used in the integration and test of the EOS-AM spacecraft and the EOSDIS Test System. The full complement of components will be first demonstrated in a prototype very low-cost ground capture and processing station for EOS direct broadcast data.

This new generation of return link processing components will help lower the cost and increase the performance of NASA's future data systems. However, return link processing is just one of many areas where high integration ASIC technology can be used to create cost effective system solutions. In the future, the DSTD will target high integration ASIC solutions to lower the cost of digital signal processing, telemetry stream simulation, and science data processing.

7. REFERENCES

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8. NOMENCLATURE

ASIC	Application-specific Integrated Circuit
CCSDS	Consultative Committee for Space Data Systems
CMOS	Complementary Metal Oxide Semiconductor
CSP	CCSDS Service Processor
DSN	Deep Space Network
DSTD	Data Systems Technology Division
FIFO	First-In, First-Out
GSFC	Goddard Space Flight Center
HST	Hubble Space Telescope
ECL	Emitter Coupled Logic
EOS	Earth Observing System
EOSDIS	Earth Observing System Data Information System
FIFO	First-In, First-Out
GaAs	Gallium Arsenide
Mbps	Megabits per second
MO&DSD	Mission Operations and Data Systems Directorate
NASA	National Aeronautics and Space Administration
PIFS	Parallel Integrated Frame Synchronizer
PLD	Programmable Logic Devices
RSEC	Reed-Solomon Error Correction
VLSI	Very Large Scale Integration